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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/647,106	08/25/2003	Andrew James Booker	550-462	9839

23117 7590 11/03/2006

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EXAMINER	
KHATRI, ANIL	
ART UNIT	**PAPER NUMBER**
2191	

DATE MAILED: 11/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/647,106	BOOKER ET AL.	
	Examiner	Art Unit	
	Anil Khatri	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/25/06* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: *"Generating Software Test Information Related To The Operation of Software Code on a Target Processor"*.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 1-26 are rejected under 35 USC 101 because they disclose a claimed invention that is an abstract idea as defined in the case *In re Warmerdam*, 33, F 3d 1354, 31 USPQ 2d 1754 (Fed. Cir. 1994).

Analysis: Claims 1-42 disclosed by the applicant as being a "method of generating software test...". Since the claims are each a series of steps to be performed on a computer the processes must be analyzed to determine whether they are statutory under 35 USC 101.

Examiner interprets that the claims 1-26 are non-statutory because claim is a computer program for processing set of instructions which capable of being executed by a method, the computer program itself is not a process and without the computer-readable medium so its functionality can be realized. Applicant submit no substance that how this will be processed without incorporating a processor, memory and medium. Therefore, claims 1-26 are generating

instruction from a sequence of instructions and executing on a processor without incorporating steps of execution in a medium. Thus, claims 1-26 are non-statutory and rejected under 35 USC 101.

II. It was noted that independent claims 27-42 are computer program product claim.

Examiner interprets that claims 27-42 are non-statutory because claim recites computer program product are program, per se i.e. the description or expressions of the program are not physical things nor are they statutory process as they do not act being performed. Computer programs do not define any structural and functional interrelationship between the computer program and other claimed aspect of the invention, which permits the computer program's functionality, could be realized. Therefore, computer program is merely a set of instructions capable of being executed by a computer, the computer program itself is not a process. Thus claims 27-42 are non-statutory and rejected under 35 USC 101.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-42 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: steps of testing software code, replacing code and steps for execution during run time etc.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Favor* USPN 5,794,063 taken with *Killian et al* USPN 6,760,888.

Regarding claims 1, 14, 27 and 35

Favor teaches,

- generating, from a sequence of instructions, at least one of which includes a condition code, a corresponding sequence of generated instructions, for selected instructions having a condition code the corresponding generated instruction being a predetermined generated instruction having a corresponding condition code (column 54, lines 10-12, "a plurality of microinstruction...");

- when during step (b) predetermined generated instruction is encountered, determining operation of target processor whether the condition code of predetermined generated instruction is satisfied and, if so, replacing predetermined generated instruction with corresponding instruction from sequence of instructions so as to cause corresponding instruction to be executed (column 32, lines 34-39, "operation fetching... misprediction"). *Favor* doesn't teaches explicitly executing, on a target processor, sequence of generated instructions.

However, *Killian et al* teaches (see summary of the invention, figures 3-6). Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to incorporate target processor to modify and fix code in different machines. The modification would have been obvious because one of ordinary skill in the art would have been motivated to combine teaching into testing process to debug the code in a target processor to reduce the size and cost of a source processor.

Regarding claims 2, 15 and 28

Favor teaches,

each instruction of said sequence of instructions includes a condition code (column 32, lines 34-39, "operation fetching... misprediction").

Regarding claims 3, 16, 29 and 36

Favor teaches,

condition code is an instruction qualifier, which prevents the instruction from being executed by target processor unless status information satisfies condition code (column 5, lines 61-67, "a branch unit...", column 7, lines 1-14, "all condition code... predicted address").

Regarding claims 4, 17 and 37

Killian et al teaches,

status information is predetermined architectural state associated with target processor and condition code specifies a status of predetermined architectural state that must be met in order for the instruction to be executed (column 7, lines 16-25, "ISA definition... develop for it).

Regarding claims 5, 13, 18, 26, 30, 38 and 42

Favor teaches,

predetermined generated instruction is an instruction, which is not recognized by target processor (column 19, lines 19-29, "the instruction look ahead... next instructions").

Regarding claims 6, 19 and 31

Favor teaches,

generating, from sequence of instructions, a sequence of generated instructions, a predetermined generated instruction being generated for each instruction in the sequence of instructions (column 54, lines 10-12, "a plurality of microinstruction...").

Regarding claims 7-9 and 32-34

Favor teaches,

- partitioning sequence of instructions into a number of instruction groups, each instruction group including one or more instructions (column 5, lines 33-40, "schedule is partitioned... execution units"); and

- generating predetermined generated instruction for one instruction in each of instruction group (column 54, lines 10-12, "a plurality of microinstruction...").

Regarding claims 10, 11, 23, 39 and 40

Favor teaches,

incrementing a coverage counter when the condition code of the predetermined generated instruction is satisfied to provide an indication that corresponding instruction will be executed (column 25, lines 22-41, "the pointers are... is addressed").

Regarding claims 12, 25 and 41

Favor teaches,

replacing a preceding instruction in sequence of generated instructions with predetermined generated instruction having a condition code corresponding to preceding instruction (column 10, lines 37-43, "the segment override... prefix").

Regarding claims 20, 21, 22, 24 and 25

Favor teaches,

instruction generation logic is operable to partition sequence of instructions into a number of instruction groups, each instruction group including one or more instructions, and to generate predetermined generated instruction for one instruction in each of instruction group (column 2, lines 29-54, "instruction code...Op sequence").

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anil Khatri whose telephone number is 571-272-3725. The examiner can normally be reached on M-F 8:30-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached on 571-272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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ANIL KHATRI
PRIMARY EXAMINER